Docket No.: 67162-024 **PATENT** 

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277

Eiichi FUKITA, et al. : Confirmation Number:

Serial No.: : Group Art Unit:

Filed: September 29, 2003 : Examiner:

For: LOGIC CIRCUIT DIAGRAM INPUT DEVICE

## **INFORMATION DISCLOSURE STATEMENT**

Mail Stop IDS Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

In a ccordance with the provisions of 3 7 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the document listed on the attached form PTO-1449. It is respectfully requested that the document be expressly considered during the prosecution of this application, and that the document be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The relevance of Japanese Unexamined Patent no. 2001-22799, is discussed in the present specification.

## Serial No.:

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: September 29, 2003

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APPLICATION												
						APPLICANT Eiichi FUKITA, et al.						
(PTO-1449)						FILING DATE GRO September 29, 2003			OUP			
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<sup>\*</sup>EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.